

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. – 2. (Canceled)

3. (Original) A ferroelectric capacitor of the type having a top electrode, a ferroelectric thin film, and a bottom electrode, characterized in that said ferroelectric thin film is a perovskite-type oxide containing a metal element, and at least either of said top electrode or said bottom electrode has a multilayer structure formed by sequentially laminating a layer containing an intermetallic compound composed of said metal element and a noble metal and a layer of said noble metal, the former being adjacent to the interface of the ferroelectric thin film.

4. (Canceled)

5. (Currently Amended) A ferroelectric capacitor as defined in Claim 3, in which said noble metal is Pt, said intermetallic compound is one which is composed of Pb and Pt, with the Pb content being 50 atom% or less, and said ~~transition metal~~ is ferroelectric capacitor further having a buffer layer comprised of Ti.

6. (Canceled)

7. (Previously Presented) A ferroelectric capacitor as defined in Claim 3, in which said intermetallic compound is one which has a $L1_2$ type crystal structure represented by the composition formula of Pt_3Pb .

8. (Previously Presented) A ferroelectric capacitor as defined in Claim 3, in which said intermetallic compound is one which has a crystal structure based on a face centered cubic lattice.

9. (Previously Presented) A ferroelectric capacitor as defined in Claim 3, in which said bottom electrode has a crystal structure based on a face centered cubic lattice and orients mainly in the (111) plane, (100) plane, or (110) plane.

10. (Previously Presented) A ferroelectric capacitor as defined in Claim 3, in which both said ferroelectric thin film and said bottom electrode orient mainly in the (111) plane, (100) plane, or (110) plane.

11. (Original) A ferroelectric capacitor of the type having a top electrode, a ferroelectric thin film, and a bottom electrode, characterized in that said bottom electrode is of double layer structure composed of a first layer of metal having a face centered cubic lattice and a second layer of an alloy containing said metal, and the difference in lattice constant between said first layer and said second layer is 3.5% or less.

12. – 13. (Canceled)

14. (Previously Presented) A ferroelectric capacitor as defined in Claim 3, in which said ferroelectric thin film has a thickness of 1000Å or less.

15. (Previously Presented) A ferroelectric memory cell in which the ferroelectric capacitor defined in Claim 3 formed on the gate of a semiconductor field effect transistor.

16. (Previously Presented) A ferroelectric memory cell in which the ferroelectric capacitor defined in Claim 3, is formed as the capacitor of the semiconductor MOS part.

17. (Previously Presented) A semiconductor device which has the ferroelectric memory cell defined in Claim 15.

18. (Previously Presented) A system LSI which has the ferroelectric memory cell defined in Claim 15.

19. (Previously Presented) An IC card which has the ferroelectric memory cell defined in Claim 15.

20. – 21. (Canceled)

22. (Previously Presented) A method of forming a ferroelectric capacitor forming a buffer layer on a substrate, said buffer layer being comprised of a transition metal or a nitride thereof;

forming a bottom electrode on said buffer layer, wherein said bottom electrode includes an intermetallic compound comprised of a metal element and a noble metal;

forming a ferroelectric thin film on said bottom electrode, wherein said ferroelectric thin film is comprised of a perovskite-type oxide containing said metal element, and

forming a top electrode on said ferroelectric thin film, wherein said top electrode is formed as a multilayer structure by sequentially laminating a layer containing an intermetallic compound comprised of said metal element and a noble metal and a layer of said noble metal, the former being adjacent to the interface of the ferroelectric thin film.

23. (Previously Presented) A semiconductor device comprised of the ferroelectric memory cell defined in Claim 16.

24. (Previously Presented) A system LSI comprised of the memory cell defined in Claim 16.

25. (Previously Presented) An IC card comprised of the ferroelectric memory cell defined in Claim 16.